

1/4 DUTY LCD DRIVER

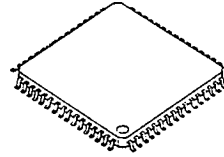
■ GENERAL DESCRIPTION

The NJU6433 is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6433 is useful for the digital tuning system or others segment type display driver.

■ PACKAGE OUTLINE

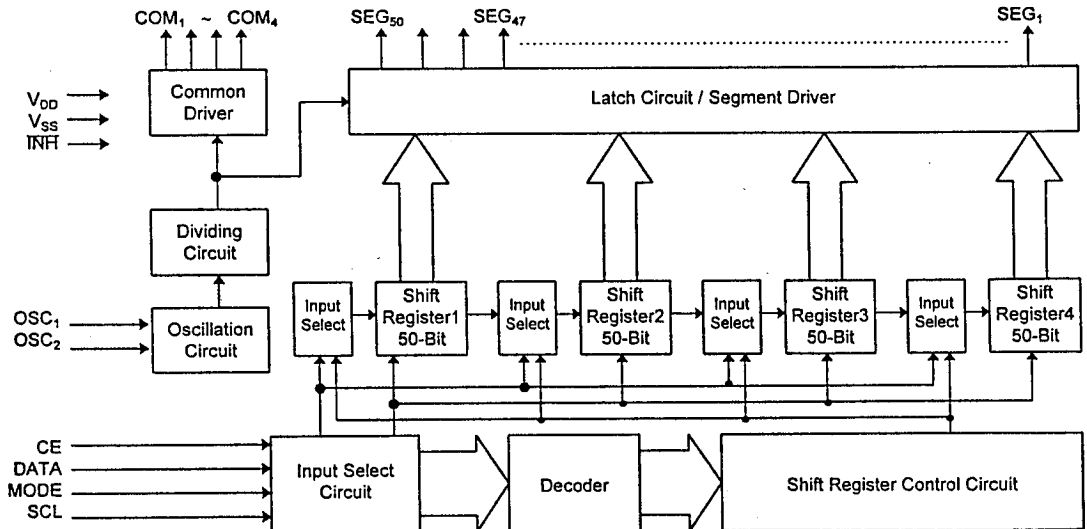


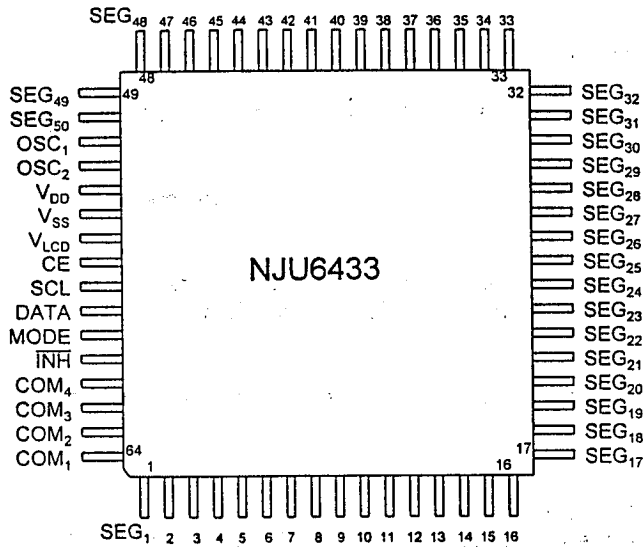
NJU6433F

■ FEATURES

- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required)
- Display Off Function (INH Terminal)
- Operating Voltage --- 2.4~5.5V
- LCD Driving Voltage --- 6.5V Max.
- Package Outline --- QFP 64 (D1, G1)
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

■ TERMINAL DESCRIPTION

| NO. | SYMBOL | F U N C T I O N |
|-------|--------------------------------------|--|
| 1~50 | SEG ₁ ~ SEG ₅₀ | LCD Segment Output Terminals |
| 51 | OSC ₁ | Oscillation Terminals : External resistance is connected to these terminals. |
| 52 | OSC ₂ | |
| 53 | V _{DD} | Power Supply (+5V) |
| 54 | V _{SS} | Power Supply (0V) |
| 55 | V _{LCD} | Power Supply for LCD Driving The relation : $V_{DD} - V_{LCD} \leq 1.3V_{DD}$, $V_{LCD} \geq V_{SS}$ must be maintained. |
| 56 | CE | Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch |
| 57 | SCL | Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge. |
| 58 | DATA | Serial Data Input Terminal Data input timing : SCL clock rise edge |
| 59 | MODE | Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (refer the mode setting table for mode setting contents) |
| 60 | $\overline{\text{INH}}$ | Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off |
| 61~64 | COM ₄ ~COM ₁ | LCD Common Output Terminals |

FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit :

The oscillation circuit operate by connecting external resistance (capacitance is incorporated).

This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(2) Data Input Format

(2-1) Input Data Correspond to Segment Status

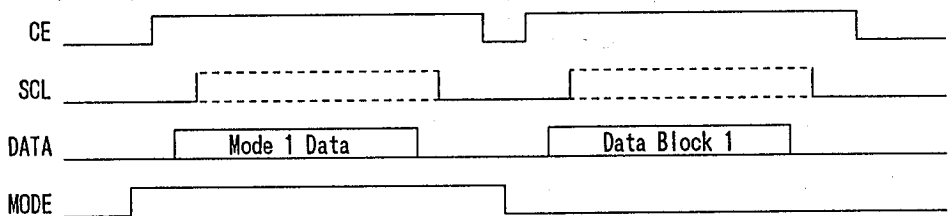
The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

| Data Dxxx | Segment Status |
|-----------|----------------|
| "H" | ON |
| "L" | OFF |

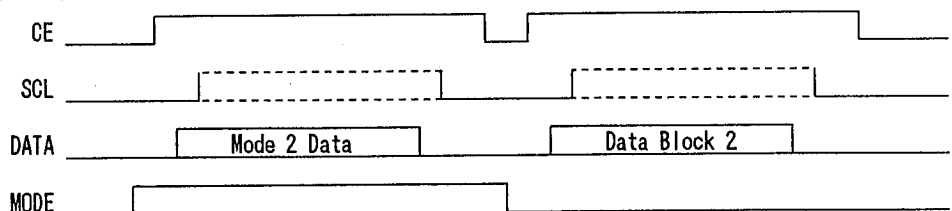
(2-2) Write to Shift-register

Write to shift-register performs Mode setting data writing and LCD display data writing.

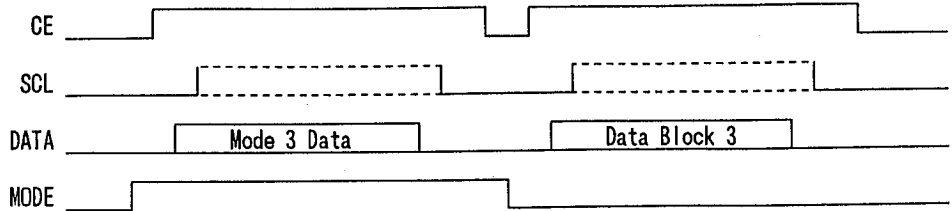
Example 1 (Mode 1): Write to Shift-register 1 (1 to 50-bit)



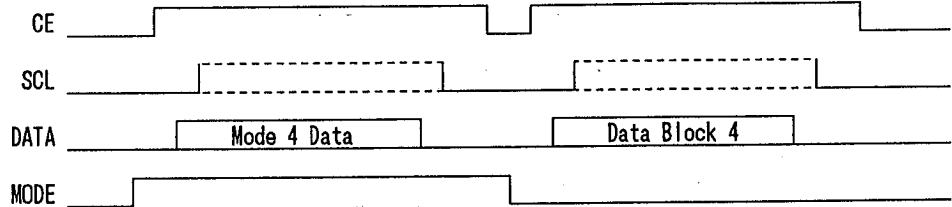
Example 2 (Mode 2): Write to Shift-register 2 (51 to 100-bit)



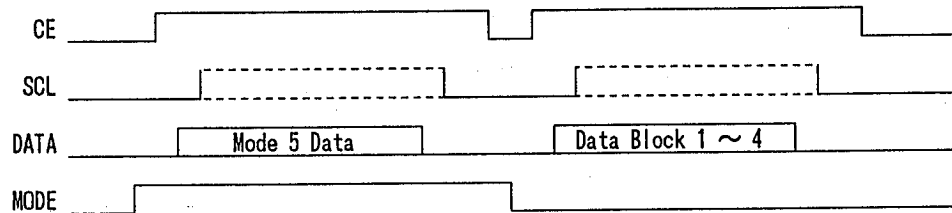
Example 3 (Mode 3): Write to Shift-register 3 (101 to 150-bit)



Example 4 (Mode 4): Write to Shift-register 4 (151 to 200-bit)

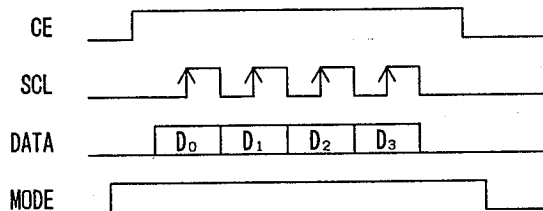


Example 5 (Mode 5): Write to Shift-register 5 (1 to 200-bit)


(2-3) Mode Setting

Transfer register selection and all clear of the shift register are performed by writing 4-bit code shown below to the decoder in CE = "H" and MODE = "H" state.

< Input Timing Chart >



< Mode Setting Table >

| CE Terminal | MODE Terminal | DATA Terminal D ₃ D ₂ D ₁ D ₀ | MODE # Data (HEX) | Mode Set Up |
|-------------|---------------|--|----------------------|--|
| "H" | "H" | 0 0 0 1 | (01 _H) | Select the shift-register 1 |
| | | 0 0 1 0 | (02 _H) | Select the shift-register 2 |
| | | 0 0 1 1 | (03 _H) | Select the shift-register 3 |
| | | 0 1 0 0 | (04 _H) | Select the shift-register 4 |
| | | 0 1 0 1 | (05 _H) | Select the all shift-register (1 to 4) |
| | | 1 1 1 1 | (0F _H) | All shift-register is "L" |

Note) The internal decoder is data through type. Therefore, the 8 bits data also can write though only 4 bits data from the CE falling are validated.

(2-5) Display Data Correspond to Segment and Common Terminals

| Mode | Data | Segment | COM ₁ | COM ₂ | COM ₃ | COM ₄ | Data Block |
|--------|--|-------------------|------------------|------------------|------------------|------------------|--------------|
| Mode 1 | D ₁ D ₂ D ₃ D ₄ | SEG ₁ | ○ | ○ | ○ | ○ | Data Block 1 |
| | D ₅ D ₆ D ₇ D ₈ | SEG ₂ | ○ | ○ | ○ | ○ | |
| | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| | D ₄₅ D ₄₆ D ₄₇ D ₄₈ | SEG ₁₂ | ○ | ○ | ○ | ○ | |
| | D ₄₉ D ₅₀ | SEG ₁₃ | ○ | ○ | | | |
| Mode 2 | D ₅₁ D ₅₂ | SEG ₁₃ | | | ○ | ○ | Data Block 2 |
| | D ₅₃ D ₅₄ D ₅₅ D ₅₆ | SEG ₁₄ | ○ | ○ | ○ | ○ | |
| | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| | D ₉₇ D ₉₈ D ₉₉ D ₁₀₀ | SEG ₂₅ | ○ | ○ | ○ | ○ | |
| Mode 3 | D ₁₀₁ D ₁₀₂ D ₁₀₃ D ₁₀₄ | SEG ₂₆ | ○ | ○ | ○ | ○ | Data Block 3 |
| | D ₁₀₅ D ₁₀₆ D ₁₀₇ D ₁₀₈ | SEG ₂₇ | ○ | ○ | ○ | ○ | |
| | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| | D ₁₄₅ D ₁₄₆ D ₁₄₇ D ₁₄₈ | SEG ₃₇ | ○ | ○ | ○ | ○ | |
| | D ₁₄₉ D ₁₅₀ | SEG ₃₈ | ○ | ○ | | | |
| Mode 4 | D ₁₅₁ D ₁₅₂ | SEG ₃₈ | | | ○ | ○ | Data Block 4 |
| | D ₁₅₃ D ₁₅₄ D ₁₅₅ D ₁₅₆ | SEG ₃₉ | ○ | ○ | ○ | ○ | |
| | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| | D ₁₉₇ D ₁₉₈ D ₁₉₉ D ₂₀₀ | SEG ₅₀ | ○ | ○ | ○ | ○ | |

■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------------|------------|----------------------------|-------------|
| Operating Voltage (1) | V_{DD} | - 0.3 ~ + 7.0 | V |
| Operating Voltage (2) Note 1) | V_{LCD} | $V_{DD} - 6.5 \sim V_{SS}$ | V |
| Input Voltage (1) Note 2) | $V_{i(1)}$ | - 0.3 ~ + 7.0 | V |
| Input Voltage (2) Note 3) | $V_{i(2)}$ | - 0.3 ~ $V_{DD}+0.3$ | V |
| Output Voltage Note 3) | V_o | - 0.3 ~ $V_{DD}+0.3$ | V |
| Output Current (1) Note 4) | $I_{o(1)}$ | 100 | μA |
| Output Current (2) Note 5) | $I_{o(2)}$ | 1.0 | mA |
| Power Dissipation | P_d | 300 | mW |
| Operating Temperature | T_{opr} | - 30 ~ + 85 | $^{\circ}C$ |
| Storage Temperature | T_{stg} | - 40 ~ + 125 | $^{\circ}C$ |

Note 1) $|V_{DD} - V_{LCD}| \leq 1.3V_{DD}$, $V_{LCD} \leq V_{SS}$

Note 2) CE, SCL, DATA, MODE, TNH Terminals

Note 3) OSC₁, OSC₂ Terminals

Note 4) SEG₁ ~ SEG₅₀ Terminals

Note 5) COM₁ ~ COM₄ Terminals

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

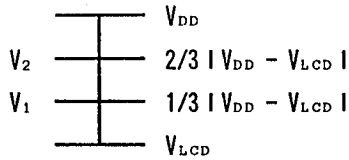
($T_a=25^{\circ}C$, $V_{DD}=5.0V$, $V_{SS}=0V$, $V_{LCD}=V_{DD}-6.5V$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|-------------|---|--------------|-------|---------------|---------|
| Operating Voltage (1) | V_{DD} | V_{DD} Terminal | 2.4 | | 5.5 | V |
| Operating Voltage (2) | V_{LCD} | V_{LCD} Terminal Note 6) | V_{SS} | | $V_{DD}-6.5$ | V |
| "H" Input Voltage | V_{IH} | CE, SCL, DATA, MODE, | 0.7 V_{DD} | | V_{DD} | V |
| "L" Input Voltage | V_{IL} | TNH Terminals | V_{SS} | | 0.3 V_{DD} | V |
| "H" Input Current | I_{IH} | CE, SCL, DATA, MODE, $V_i=V_{DD}$ | | | 5.0 | μA |
| "L" Input Current | I_{IL} | TNH Terminals $V_i=V_{SS}$ | | | 5.0 | μA |
| "H" Output Voltage (1) | $V_{OH(1)}$ | SEG ₁ ~SEG ₅₀ $I_o=-10\mu A$ | $V_{DD}-1.0$ | | | V |
| "L" Output Voltage (1) | $V_{OL(1)}$ | $I_o=+10\mu A$ | | | $V_{LCD}+1.0$ | V |
| Middle Level Voltage 1/3 (1) | $V_{MS1/3}$ | SEG ₁ ~SEG ₅₀ $I_o=\pm 10\mu A$ | $V_1-1.0$ | V_1 | $V_1+1.0$ | V |
| Middle Level Voltage 2/3 (1) | $V_{MS2/3}$ | Note 7) $I_o=\pm 10\mu A$ | $V_2-1.0$ | V_2 | $V_2+1.0$ | V |
| "H" Output Voltage (2) | $V_{OH(2)}$ | COM ₁ ~COM ₄ $I_o=-100\mu A$ | $V_{DD}-0.6$ | | | V |
| "L" Output Voltage (2) | $V_{OL(2)}$ | $I_o=+100\mu A$ | | | $V_{LCD}-0.6$ | V |
| Middle Level Voltage 1/3 (2) | $V_{MC1/3}$ | COM ₁ ~COM ₄ $I_o=\pm 100\mu A$ | $V_1-0.6$ | V_1 | $V_1+0.6$ | V |
| Middle Level Voltage 2/3 (2) | $V_{MC2/3}$ | Note 7) $I_o=\pm 100\mu A$ | $V_2-0.6$ | V_2 | $V_2+0.6$ | V |
| Oscillating Frequency Range | f_{osc} | OSC ₁ , OSC ₂ Terminals | 25 | | 200 | kHz |
| Oscillating Frequency | f_{osc} | R=140k Ω | 115 | 130 | 145 | kHz |
| Operating Current (1) | I_{DD} | V_{DD} Terminal | | 50 | 80 | μA |
| Operating Current (2) | I_{LCD} | V_{LCD} Terminal | | 15 | | μA |
| Hysteresis Voltage | V_H | CE, SCL, DATA, MODE, TNH Terminals | 0.3 | | | V |

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Note 6) The relation: $|V_{DD} - V_{LCD}| \leq 1.3V_{DD}$, $V_{LCD} \leq V_{SS}$ must be maintained.

Note 7) $V_1 = 1/3 |V_{DD} - V_{LCD}|$, $V_2 = 2/3 |V_{DD} - V_{LCD}|$

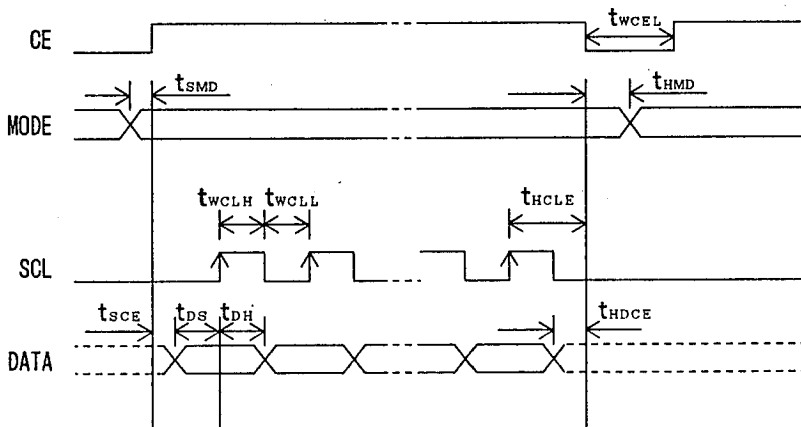


• AC Characteristics

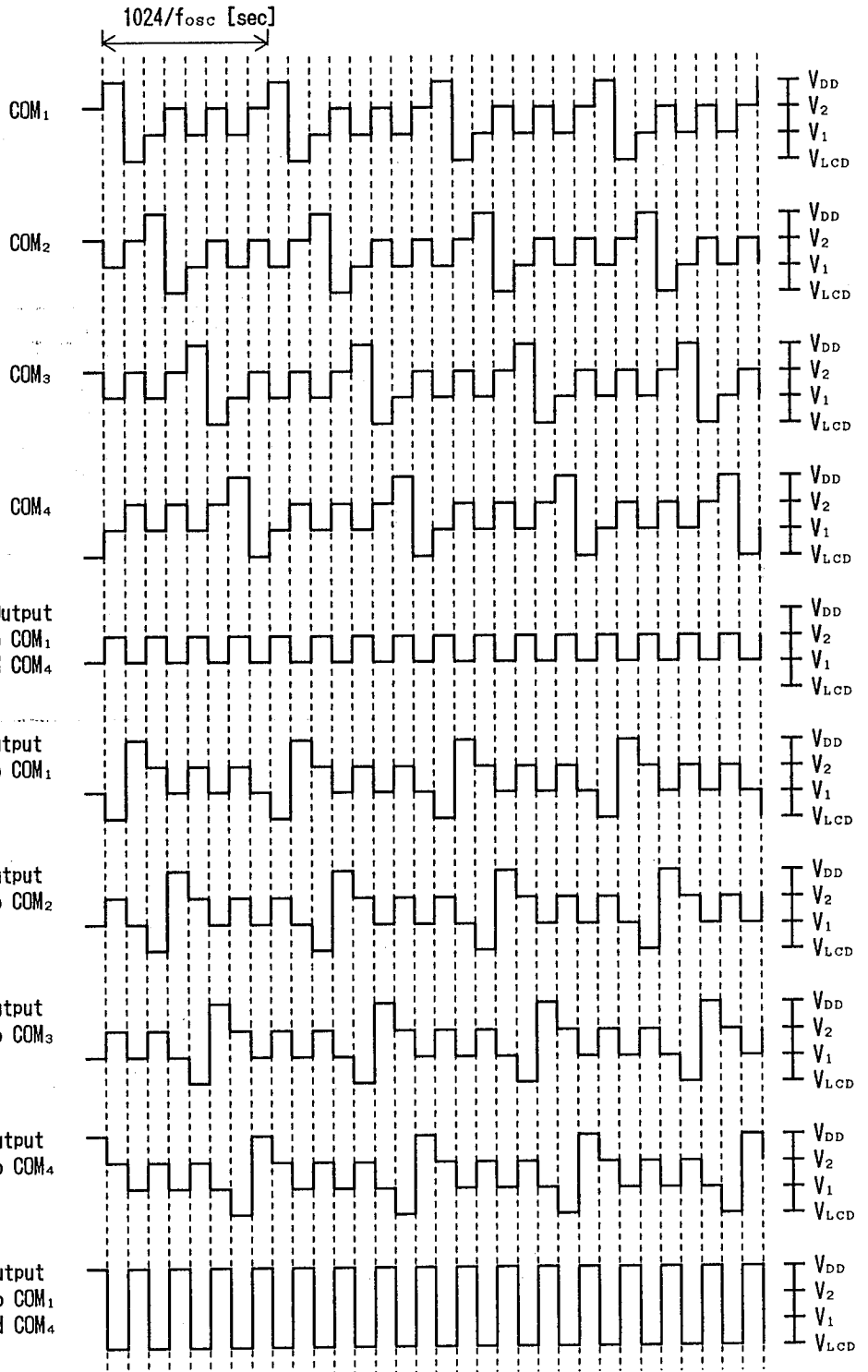
($T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$, $V_{SS}=0\text{V}$, $V_{LCD}=V_{DD}-6.5\text{V}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|------------|---------------------|------|-----|-----|---------------|
| "L" Clock Pulse Width | t_{WCLL} | SCL Terminal | 0.25 | | | μs |
| "H" Clock Pulse Width | t_{WCLH} | | 0.25 | | | μs |
| Data Set-up Time | t_{DS} | SCL, DATA Terminals | 0.25 | | | μs |
| Data Hold Time | t_{DH} | | 0.25 | | | μs |
| CE Set-up Time | t_{SCE} | CE, DATA Terminals | 1.0 | | | μs |
| CE Hold Time (1) | t_{HDCE} | | 1.0 | | | μs |
| CE Hold Time (2) | t_{HCLE} | CE, SCL Terminals | 1.25 | | | μs |
| Mode Set-up Time | t_{SMD} | CE, MODE Terminals | 0.25 | | | μs |
| Mode Hold Time | t_{HMD} | | 0.25 | | | μs |
| "L" Chip Enable Pulse Width | t_{WCEL} | CE Terminal | 4.0 | | | μs |

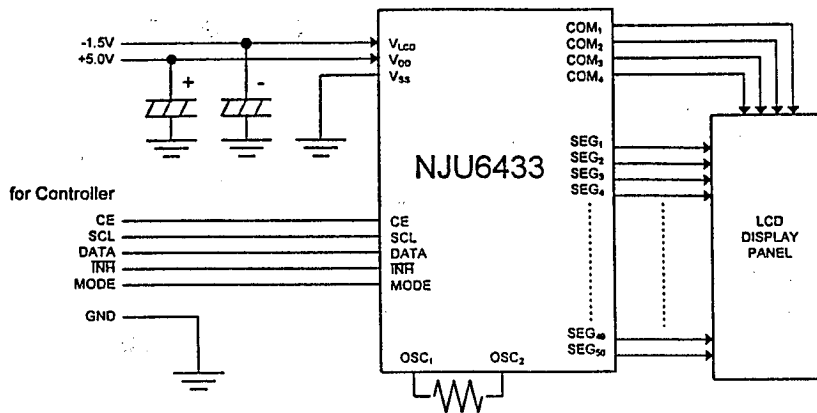
• Input Timing Characteristics



■ LCD Driving Waveform(1/4DUTY · 1/3BIAS)



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APPLICATION CIRCUIT


(Note) The internal display data is undefined when V_{DD} is just turned on.

To avoid the meaningless display, please keep the \overline{TNH} terminal at "L" until proper display data has been transferred.

In order to set the initial condition, 200-bit blank data or the first 200-bit data to be displayed should be transferred.

MEMO

[CAUTION]

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