

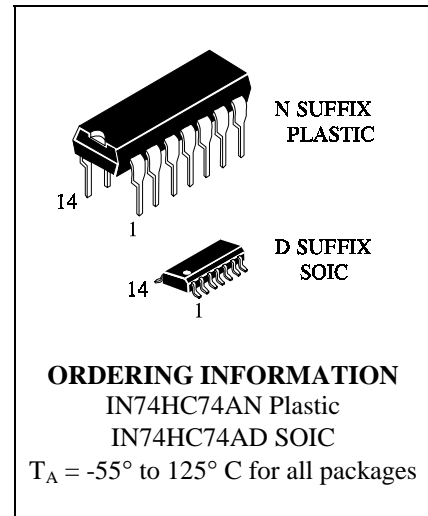
IN74HC74A

**Dual D Flip-Flop with Set and Reset
High-Performance Silicon-Gate CMOS**

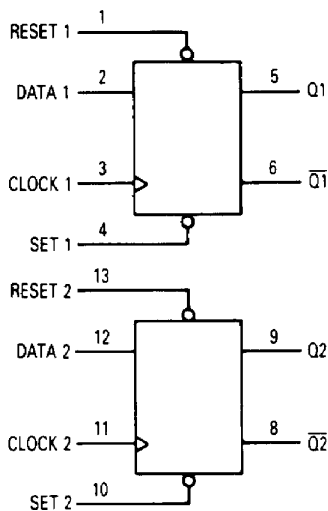
The IN74HC74A is identical in pinout to the LS/ALS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

RESET 1	1 ●	14	V_{CC}
DATA 1	2	13	RESET 2
CLOCK 1	3	12	DATA 2
SET 1	4	11	CLOCK 2
Q1	5	10	SET 2
$\bar{Q}1$	6	9	Q2
GND	7	8	$\bar{Q}2$

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H		H	H	L
H	H		L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H		X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} = 2.0 V	0	1000	ns
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	2.0	20	80	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or Q̄ (Figures 1 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or Q̄ (Figures 2 and 4)	2.0	105	130	160	ns
		4.5	21	26	32	
		6.0	18	22	27	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)	Typical @25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	39			

TIMING REQUIREMENTS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	3.0	3.0	3.0	ns
		4.5	3.0	3.0	3.0	
		6.0	3.0	3.0	3.0	
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	8.0	8.0	8.0	ns
		4.5	8.0	8.0	8.0	
		6.0	8.0	8.0	8.0	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

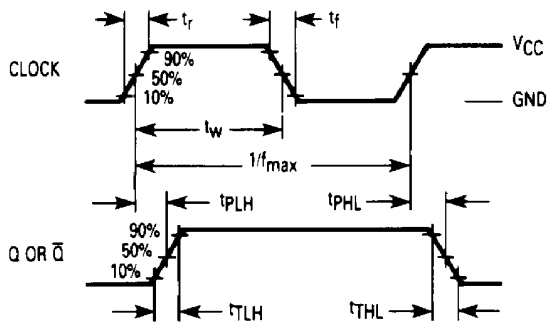


Figure 1. Switching Waveform

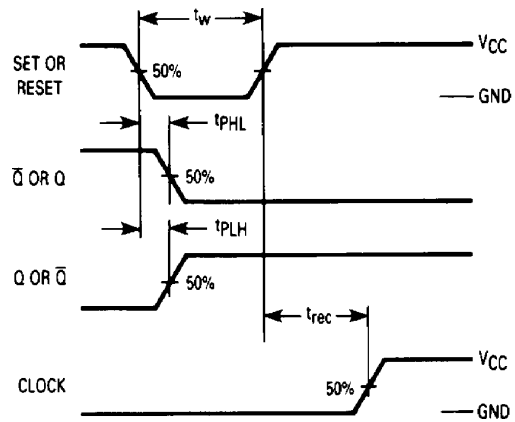


Figure 2. Switching Waveform

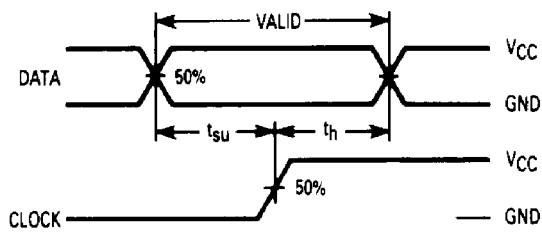
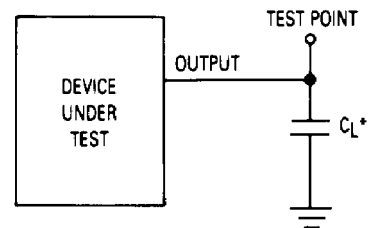


Figure 3. Switching Waveform



*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

