**FAIRCHILD**
SEMICONDUCTOR™

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# 74LCX16500
# Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

## General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LCX16500 is designed for low voltage (2.5V or 3.3V) $V_{CC}$ applications with the capability of interfacing to a 5V signal environment.

The LCX16500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power.

## Features

■ 5V tolerant inputs and outputs

■ 2.3V–3.6V $V_{CC}$ specifications provided

■ 6.0 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 20 µA $I_{CC}$ max

■ Power down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA output drive ($V_{CC}$ = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

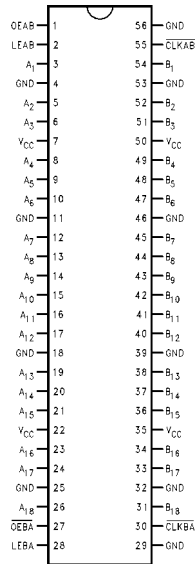■ ESD performance:
   Human body model > 2000V
   Machine model > 200V

**Note 1:** To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ and OE tied to GND through a resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX16500MEA | MS56A | 56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LCX16500MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

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**74LCX16500**

## Connection Diagram

```
OEAB    ┌ 1      56 ┐ GND
LEAB    ┌ 2      55 ┐ CLKAB
A1      ┌ 3      54 ┐ B1
GND     ┌ 4      53 ┐ GND
A2      ┌ 5      52 ┐ B2
A3      ┌ 6      51 ┐ B3
VCC     ┌ 7      50 ┐ VCC
A4      ┌ 8      49 ┐ B4
A5      ┌ 9      48 ┐ B5
A6      ┌ 10     47 ┐ B6
GND     ┌ 11     46 ┐ GND
A7      ┌ 12     45 ┐ B7
A8      ┌ 13     44 ┐ B8
A9      ┌ 14     43 ┐ B9
A10     ┌ 15     42 ┐ B10
A11     ┌ 16     41 ┐ B11
A12     ┌ 17     40 ┐ B12
GND     ┌ 18     39 ┐ GND
A13     ┌ 19     38 ┐ B13
A14     ┌ 20     37 ┐ B14
A15     ┌ 21     36 ┐ B15
VCC     ┌ 22     35 ┐ VCC
A16     ┌ 23     34 ┐ B16
A17     ┌ 24     33 ┐ B17
GND     ┌ 25     32 ┐ GND
A18     ┌ 26     31 ┐ B18
OEBA    ┌ 27     30 ┐ CLKBA
LEBA    ┌ 28     29 ┐ GND
```

## Truth Table (Note 2)

| Inputs | | | | Output |
|---|---|---|---|---|
| OEAB | LEAB | $\overline{CLKAB}$ | $A_n$ | $B_n$ |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↓ | L | L |
| H | L | ↓ | H | H |
| H | L | H | X | $B_0$ (Note 3) |
| H | L | L | X | $B_0$ (Note 4) |

**Note 2:** A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

**Note 3:** Output level before the indicated steady-state input conditions were established.

**Note 4:** Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
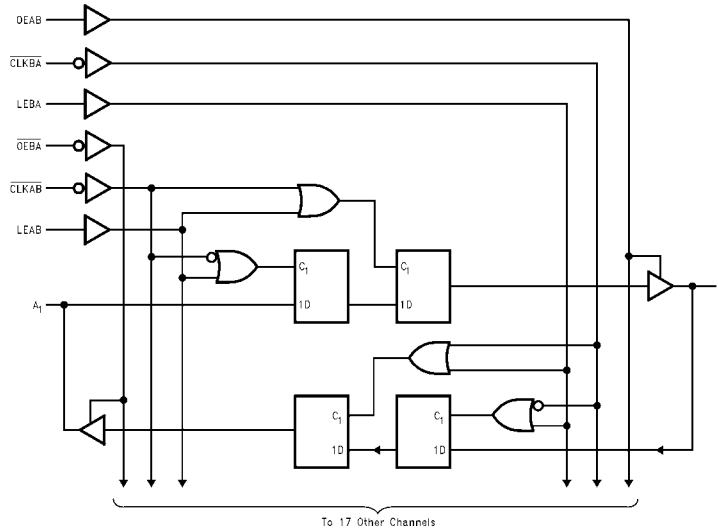
## Functional Description

For A-to-B data flow, the LCX16500 operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. Output-enable OEAB is active-HIGH. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active HIGH and $\overline{OEBA}$ is active LOW).

## Logic Diagram



To 17 Other Channels

## Absolute Maximum Ratings(Note 5)

| Symbol | Parameter | Value | Conditions | Units |
|--------|-----------|-------|------------|-------|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | −0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | −0.5 to +7.0 | Output in 3-STATE | V |
| | | −0.5 to $V_{CC}$ + 0.5 | Output in HIGH or LOW State (Note 6) | |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O$ < GND | mA |
| | | +50 | $V_O$ > $V_{CC}$ | |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

## Recommended Operating Conditions (Note 7)

| Symbol | Parameter | | Min | Max | Units |
|--------|-----------|--|-----|-----|-------|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V – 3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V – 3.0V | | ±12 | |
| | | $V_{CC}$ = 2.3V – 2.7V | | ±8 | |
| $T_A$ | Free-Air Operating Temperature | | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 5:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 6:** $I_O$ Absolute Maximum Rating must be observed.

**Note 7:** Unused (inputs or I/O's) must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C | | Units |
|--------|-----------|------------|--------------|-----|-----|-------|
| | | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2.3 – 2.7 | 1.7 | | V |
| | | | 2.7 – 3.6 | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | | 2.3 – 2.7 | | 0.7 | V |
| | | | 2.7 – 3.6 | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 µA | 2.3 – 3.6 | $V_{CC}$ – 0.2 | | V |
| | | $I_{OH}$ = −8 mA | 2.3 | 1.8 | | |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 µA | 2.3 – 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 8 mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | $0 \le V_I \le 5.5V$ | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE I/O Leakage | $0 \le V_O \le 5.5V$ | 2.3 – 3.6 | | ±5.0 | µA |
| | | $V_I = V_{IH}$ or $V_{IL}$ | | | | |
| $I_{OFF}$ | Power-Off Leakage Current | $V_I$ or $V_O$ = 5.5V | 0 | | 10 | µA |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | V_CC (V) | T_A = −40°C to +85°C | | Units |
|--------|-----------|-----------|----------|-----|-----|-------|
| | | | | Min | Max | |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.3 – 3.6 | | 20 | μA |
| | | $3.6V \leq V_I, V_O \leq 5.5V$ (Note 8) | 2.3 – 3.6 | | ±20 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} -0.6V$ | 2.3 – 3.6 | | 500 | μA |

**Note 8:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$ | | | | | | Units |
|--------|-----------|------|------|------|------|------|------|-------|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 2.5V \pm 0.2V$ | | |
| | | $C_L = 50$ pF | | $C_L = 50$ pF | | $C_L = 30$ pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 170 | | | | | | MHz |
| $t_{PHL}$ | Propagation Delay | 1.5 | 6.0 | 1.5 | 7.0 | 1.5 | 7.2 | ns |
| $t_{PLH}$ | Bus to Bus | 1.5 | 6.0 | 1.5 | 7.0 | 1.5 | 7.2 | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 6.7 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| $t_{PLH}$ | Clock to Bus | 1.5 | 6.7 | 1.5 | 8.0 | 1.5 | 8.4 | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| $t_{PLH}$ | LE to Bus | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | |
| $t_{PZL}$ | Output Enable Time | 1.5 | 7.2 | 1.5 | 8.2 | 1.5 | 9.4 | ns |
| $t_{PZH}$ | | 1.5 | 7.2 | 1.5 | 8.2 | 1.5 | 9.4 | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| $t_{PHZ}$ | | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | |
| $t_S$ | Setup Time | 2.5 | | 2.5 | | 3.0 | | ns |
| $t_H$ | Hold Time | 1.5 | | 1.5 | | 2.0 | | ns |
| $t_W$ | Pulse Width | 3.0 | | 3.0 | | 3.5 | | ns |
| $t_{OSHL}$ | Output to Output Skew | | 1.0 | | | | | ns |
| $t_{OSLH}$ | (Note 9) | | 1.0 | | | | | |

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$), or LOW-to-HIGH ($t_{OSLH}$).

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | V_CC (V) | T_A = 25°C Typical | Units |
|--------|-----------|-----------|----------|--------|-------|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | 0.6 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | −0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | −0.6 | |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|--------|-----------|-----------|---------|-------|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 20 | pF |

## AC LOADING and WAVEFORMS Generic for LCX Family
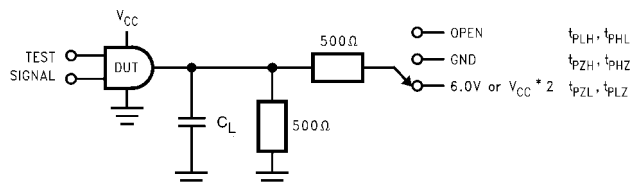


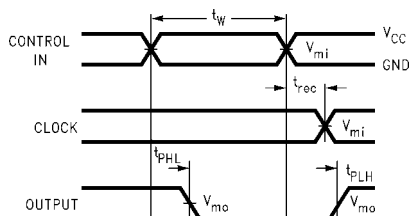FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)

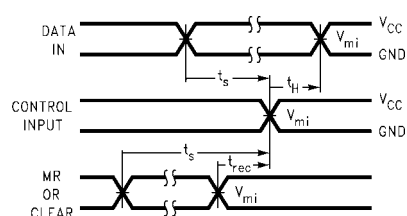| Test | Switch |
|------|--------|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC} = 3.3 \pm 0.3V$<br>$V_{CC}$ x 2 at $V_{CC} = 2.5 \pm 0.2V$ |
| $t_{PZH}$, $t_{PHZ}$ | GND |
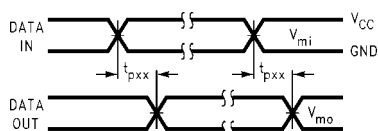


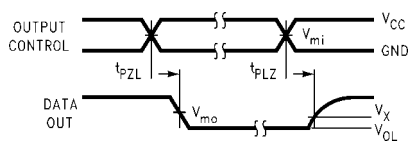**Waveform for Inverting and Non-Inverting Functions**
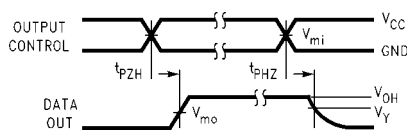


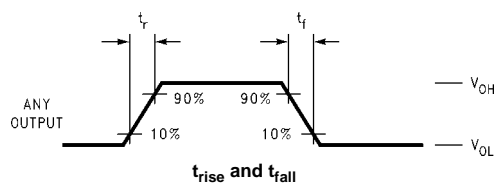**3-STATE Output High Enable and Disable Times for Logic**



**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**



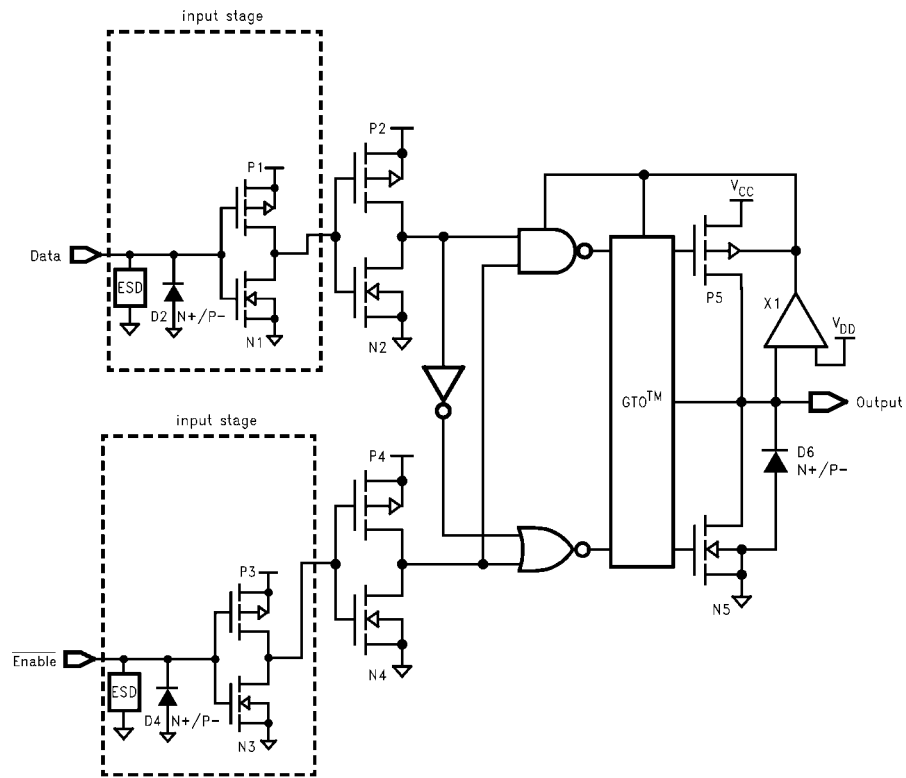**Setup Time, Hold Time and Recovery Time for Logic**



**3-STATE Output Low Enable and Disable Times for Logic**



**$t_{rise}$ and $t_{fall}$**

**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_R = t_F = 3ns$)**

| Symbol | $V_{CC}$ | | |
|--------|----------|---|---|
| | 3.3V ± 0.3V | 2.7V | 2.5V ± 0.2V |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}/2$ |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}/2$ |
| $V_x$ | $V_{OL} + 0.3V$ | $V_{OL} + 0.3V$ | $V_{OL} + 0.15V$ |
| $V_y$ | $V_{OH} - 0.3V$ | $V_{OH} - 0.3V$ | $V_{OH} - 0.15V$ |

## Schematic Diagram Generic for LCX Family

# Physical Dimensions inches (millimeters) unless otherwise noted

0.720 – 0.730
[18.30 – 18.54]
– A –

56                    29

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]
⊕ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1                    28

0.020 ±0.003
[0.51 ±0.08] TYP

0.025
[0.635] TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⊕ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –

0.025
[0.635] TYP

0.010
[0.25] MIN TYP

– C –

0° – 8° TYP

⌂ 0.004[0.10]

MS56A (REV E)
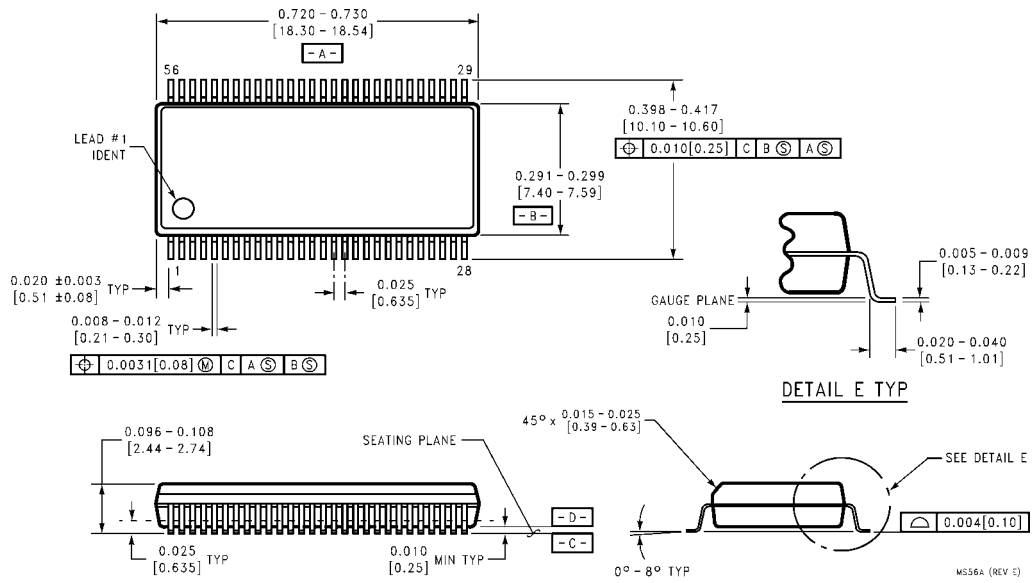
**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS56A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

MTD56 (REV B)
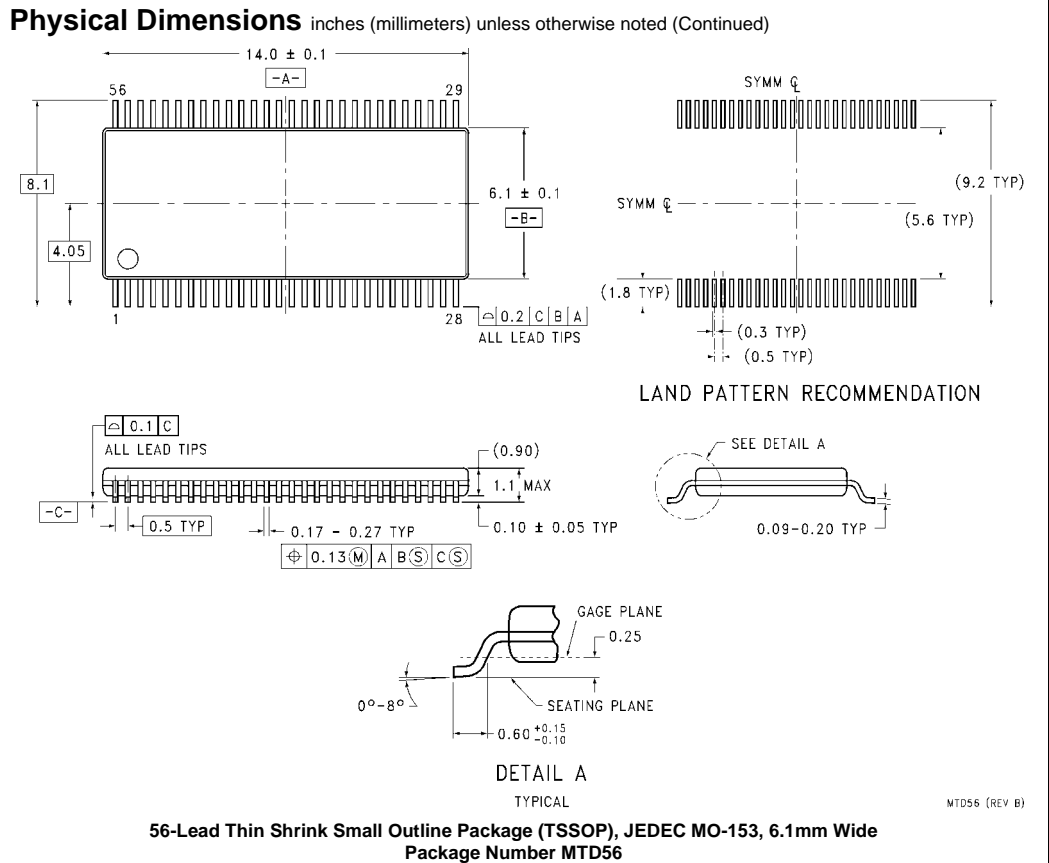
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